We claim:

1. An apparatus comprising:

an execution core;

a scan chain to transfer data to one or more nodes of the execution core; and

a reset module to provide a bit pattern to the scan chain, responsive to a reset signal.

2. The apparatus of claim 1, wherein the execution core includes first and second execution cores to be operated in FRC mode, and wherein the scan chain includes first and second scan chains corresponding to the first and second execution cores, respectively.

3. The apparatus of claim 2, wherein the reset module provides an identical bit pattern to the first and second scan chains, responsive to the reset signal.

4. The apparatus of claim 3, wherein the reset module drives the first and second scan chains in parallel.

5. The apparatus of claim 1, wherein the reset module further comprises:

a clock mux to provide a first or second clock signal to the scan chain, responsive to a reset signal; and

a pattern generator to store the bit pattern and to provide the bit patter to the scan chain, responsive to the reset signal.

6. The apparatus of claim 5, wherein the reset module further comprises a mode selector to assert a signal to the clock mux and the pattern generator, responsive to assertion of the reset signal.

7. The apparatus of claim 1, further comprising a reset tree to propagate voltage states to selected nodes of the execution core, responsive to the reset signal.

8. The apparatus of claim 1, further comprising a storage device to store a reset code module, the reset code module to step the execution core through a sequence of operations to establish states for additional nodes of the execution core.

9. A method for resetting a processor comprising:

detecting a reset event;

applying a bit pattern to a scan chain of the processor, the bit patter to drive specified states to one or more processor nodes accessible through the scan chain.

10. The method of claim 9, wherein applying the bit pattern comprises:

applying a scan clock to a clock line of the scan chain; and

applying the bit pattern to a data line of the scan chain.

11. The method of claim 9, further comprising propagating the reset signal to selected nodes of the processor through a reset tree.

12. The processor of claim 11, further comprising executing a reset code module to place additional nodes of the processor into specified states.

13. The method of claim 9 wherein the processor includes multiple execution cores to operate in FRC mode and wherein applying the bit pattern to the scan chain comprises applying the bit pattern to a corresponding scan chain in each of the execution cores.

14. The method of claim 11, wherein applying the bit pattern to a corresponding scan chain in each execution core comprises applying the bit pattern in parallel to the corresponding scan chains.

15. The method of claim 9, further comprising detecting an operating mode for the processor.

16. The method of claim 15, wherein detecting the operating mode comprises determining if the operating mode is a high performance mode or a high reliability mode, and applying a bit

pattern to the scan chain comprises applying a bit pattern to the scan chain if the determined mode is the high reliability mode.

17. A system comprising:

first and second execution cores to be operated in an FRC mode, responsive to a mode bit, each of the execution cores including a scan chain to transfer data to a first set of nodes of the execution core;

an FRC checker to be activated in FRC mode to compare data from the first and second execution cores; and

a reset module to apply a bit pattern to the scan chains of the first and second execution cores, responsive to a reset event in the system.

18. The system of claim 17, wherein the reset module includes a pattern generator to drive the bit pattern on data lines of the scan chains of the first and second execution cores responsive to a scan clock.

19. The system of claim 18, further comprising a reset tree, the reset tree including electrical connections to a second set of nodes to drive the second set of nodes to specified states responsive to the reset event.

20. The system of claim 18, further comprising a storage device to store a reset code module, the reset code module to be executed by the first and second execution cores to drive a third set of nodes to specified states, responsive to the reset event.

21. The system of claim 20, wherein first, second and third sets of nodes are mutually exclusive.

22. An apparatus comprising:

an execution core including a set of voltage nodes coupled through data and clock lines;

a reset module to drive a data signal and a clock signal to the set of voltage nodes, responsive to occurrence of a reset event, the data signal to place the voltage nodes of the set in specified logic states.

23. The apparatus of claim 22, wherein the execution core comprises first and second execution cores, each having a set of voltage nodes coupled through clock and data lines, the first and second execution cores to be operated in an FRC mode.

24. The apparatus of claim 23, wherein the data signal driven by the reset module is a bit pattern that places the set of voltage nodes of the first and second execution cores in the specified logic states.

25. The apparatus of claim 24, wherein the reset module drives the set of voltage nodes of the first and second execution cores in parallel.

26. The apparatus of claim 22, wherein the execution core comprises first and second execution cores, each having a set of voltage nodes, the first and second execution cores to be operated in an FRC mode, responsive to a mode bit being in a first state.

27. The apparatus of claim 26, wherein the reset module is disabled and the execution cores are operated in a non-FRC mode, responsive to the mode bit being in a second state.

28. The apparatus of claim 22, further comprising a reset tree to drive a second set of voltage nodes of the apparatus to second logic states, responsive to occurrence of a reset event.

29. The apparatus of claim 28 further comprising a storage device to store a reset code module, the reset code module to be executed by the execution core to place a third set of voltage nodes in specified logic states, responsive to the reset event.

30. The apparatus of claim 29, wherein the reset module establishes specified logic states for the first set of voltage nodes before the reset code module is executed.